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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/716,499	11/20/2003	Koji Mametsuka	245771US2S	6695

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EXAMINER	
SHERMAN, STEPHEN G	
ART UNIT	**PAPER NUMBER**
2629	

DATE MAILED: 11/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/716,499	MAMETSUKA, KOJI	
	Examiner	Art Unit	
	Stephen G. Sherman	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 September 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the amendment filed the 11 September 2006. Claims 1-5 are pending.

Response to Arguments

2. Applicant's arguments filed the 11 September 2006 have been fully considered but they are not persuasive.

On page 2 of the applicant's remarks the applicant begins their argument traversing the rejection of claims 1-5 under 35 U.S.C. 103 over Goto in view of Ishizuka et al. In the fourth paragraph on page 2 the applicant explains that Goto discloses a reset circuit, however, Goto does not disclose or suggest the claimed "reset signal supply section." Then in the fifth paragraph on page 2 the applicant explains that Ishizuka does not cure the deficiencies of Goto because Ishizuka discloses a reset driving method that accelerates the rise time of light emission, where electric charge stored in the luminous elements are discharged as a reset operation performed prior to the driving of the luminous elements by voltages between the anode and cathode lines arranged in a lattice shape on a simple matrix display panel. The applicant continues in the next paragraph to state that in Ishizuka the display panel does not require drive control elements, such as in the claimed invention, and that the offset voltages VR, VG, and VB are applied to the red, green, and blue luminous elements without any intention

to cancel variations in the threshold voltage Vth of each of the drive control elements, and thus "it is apparent that the offset voltages VR, VG, and VB in Ishizuka are not equivalent to the rest signals of the claimed invention." The examiner respectfully disagrees.

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

As stated in the rejection of claim 1, Goto is not used to teach of a reset signal supply section that supplies to the pixels different rest signals associated with the main wavelengths of light. Instead Ishizuka et al. was used to teach the feature. The applicant states that the rest signals of Ishizuka are different from those of the claimed invention, however, Ishizuka was only used to teach of a reset signal supply section that supplies to the pixels different rest signals associated with the main wavelengths of light to be emitted from luminous elements. The examiner never stated that the reset signals of Ishizuka intended to cancel variations in the threshold voltage of each of the drive control elements. Instead, as stated in the rejection of claim 1, Goto was used to teach of a capacitor (Fig. 9, capacitor 48a), which is connected to a control terminal of said drive control element (Fig. 9), and that temporarily stores the potential difference between the threshold voltage of said drive control element and a reset signal (see col. 7, lines 44-49, where there is a reset circuit 48 described which indicates the presence

of a reset signal, and given the arrangement of capacitor 48a and element 45, the capacitor must store the potential difference between a reset signal and the threshold voltage of element 45).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Goto (US 6,829,023) in view of Ishizuka et al. (US 6,707,438).

Regarding claim 1, Goto teaches a display device comprising:

an array section having a plurality of pixels arrayed in a matrix (Fig. 5),

each pixel (Fig. 9 shows a second embodiment of the pixels in Fig. 5) including

a luminous element (Fig. 9, element 46),

a drive control element (Fig. 9, element 45) that causes a current to flow in said luminous element according to a pixel video signal (see col. 7, lines 43-44),

a capacitor (Fig. 9, capacitor 48a), which is connected to a control terminal of said drive control element (Fig. 9), and that temporarily stores the potential difference

between the threshold voltage of said drive control element and a reset signal (see col. 7, lines 44-49, where there is a reset circuit 48 described which indicates the presence of a reset signal, and given the arrangement of capacitor 48a and element 45, the capacitor must store the potential difference between a reset signal and the threshold voltage of element 45), and

a pixel switch (Fig. 9, switch 44, see col. 7, line 43) connected via said capacitor to the control terminal of the drive control element (Fig. 9).

Goto fails to teach a reset signal supply section that supplies to the pixels different reset signals associated with the main wavelengths of light to be emitted from the luminous elements.

Ishizuka et al. disclose a reset signal supply section that supplies to the pixels different reset signals associated with the main wavelengths of light to be emitted from the luminous elements (see Figs. 8-9, and see col. 10, lines 27-41, where there is a reset signal supply section supplying a separate reset signal line for each color pixel, where each color pixel is a pixel for emitting a different wavelength of light).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Ishizuka et al. in the device of Goto to supply different reset signals according to the different color sub-pixels in a display device in order to account for the variations in the EL elements for the red, green, and blue colors (see Ishizuka, col. 5, lines 39-43).

Regarding claim 2, Goto and Ishizuka et al. disclose the display device according to claim 1.

Ishizuka et al. also disclose a device wherein the reset signal supply section is configured to output an independently-variable potential as at least one of the reset signals (see col. 9, lines 1-4, and col. 10, lines 33-42, where the variable voltage sources 18 provide the offset voltage which is the volgate provided in response to the reset signal).

Regarding claim 3, Goto and Ishizuka et al. disclose the display device according to claim 1.

Goto also discloses a device wherein said pixel includes a reset switch (Fig. 9, switch 44) that causes the reset signal to be supplied to said capacitor (see col. 7, lines 41-42, where switch 44 is providing the reset signal to the capacitor when the reset signal is supplied).

Regarding claim 4, Goto and Ishizuka et al. disclose the display device according to claim 1.

Ishizuka et al. also disclose a device wherein individual wiring-lines (Fig. 8, wiring lines A1R, A1G, and A1B) are disposed to supply the reset signals to the pixels for the respective main wavelengths (Fig. 8, where lines A1R, A1G, and A1B are the lines providing the offset voltages, or reset signal voltages as discussed above, 181R, 181G, and 181B to the pixels for the respective colors, or wavelengths).

Regarding claim 5, Goto and Ishizuka et al. disclose the display device according to claim 1.

Goto also discloses a method of driving a display device having a plurality of pixels (Fig. 5), each pixel (Fig. 9 shows a second embodiment of the pixels in Fig. 5) including a luminous element (Fig. 9, element 46), a drive control element (Fig. 9, element 45) connected in series with said luminous element (Fig. 9) and a pixel switch (Fig. 9, switch 44) connected via a capacitor (Fig. 9, capacitor 48a) to a control terminal of said-drive control element, comprising:

applying a potential equal to the threshold voltage of said drive control element to one of electrodes of said capacitor (Fig. 9, where given the arrangement shown one of the electrodes of the capacitor 48a must hold the threshold voltage of element 45 at one of its electrodes when switch 48b is closed); and supplying a pixel video signal to the other electrode of said capacitor via said pixel switch in a state where said capacitor stores the potential difference between a reset signal and the threshold voltage (see col. 7, lines 44-49, where there is a reset circuit 48 described which indicates the presence of a reset signal, and given the arrangement of capacitor 48a and element 45, the capacitor must store the potential difference between a reset signal and the threshold voltage of element 45, and then there is also a video signal described that must be supplied following the application of a reset signal).

Goto fails to teach supplying to the other electrode of said capacitor a reset signal associated with the main wavelength of light to be emitted from said luminous element.

Ishizuka et al. disclose of supplying to the column line of a pixel a reset signal associated with the main wavelength of light to be emitted from said luminous element (see Figs. 8-9, and see col. 10, lines 27-41, where there is a reset signal supply section supplying a separate reset signal line for each color pixel, where each color pixel is a pixel for emitting a different wavelength of light).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Ishizuka et al. in the device of Goto to supply different reset signals according to the different color sub-pixels in a display device in order to account for the variations in the EL elements for the red, green, and blue colors (see Ishizuka, col. 5, lines 39-43).

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen G. Sherman whose telephone number is (571) 272-2941. The examiner can normally be reached on M-F, 8:00 a.m. - 4:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SS

20 November 2006

AMR A. AWAD
SUPERVISORY PATENT EXAMINER